

FORM PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION (Use several sheets if necessary)					Docket Number (Optional): JETS-02		Application Number:					
					Applicant: Uri Cohen							
					Filing Date: 10/17/2003		Group Art Unit:					
U.S. PATENT DOCUMENTS												
EXAMINER INITIAL	DOCUMENT NUMBER							DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
NW	3	6	5	2	4	4	2	03/28/72	Powers et al.	204	273	
	3	7	4	3	5	9	0	07/03/73	Roll	204	212	
	3	9	6	3	5	8	8	06/15/76	Glenn	204	16	
	4	1	0	2	7	5	6	07/25/78	Castellani et al.	204	43	
	4	2	6	7	0	2	4	05/12/81	Weiskopf et al.	204	15	
	4	2	7	9	7	0	7	07/21/81	Anderson et al.	204	43	
	4	3	0	4	6	4	1	12/08/81	Grandia et al.	204	23	
	4	3	5	9	3	7	5	11/16/82	Smith	204	212	
	4	3	6	4	8	0	1	12/21/82	Salama	204	15	
NW	4	5	0	0	3	9	4	02/19/85	Rizzo	204	15	
FOREIGN PATENT DOCUMENTS												
	DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUBCLASS	Translation YES NO
NON-PATENT LITERATURE DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)												
NW	1	M. Matlosz, "Competitive Adsorption Effects in the Electrodeposition of Iron-Nickel Alloys", J. Electrochem. Soc. Vol. 140(8), August 1993, pp. 2272-2279.										
NW	2.	P. C. Andricacos et al., "Electrodeposition of Nickel-Iron Alloys", J. Electrochem. Soc. Vol 136(5), May 1989, pp. 1336-1340.										
NW	3	A. R. DESPIC and K. I. POPOV, "Transport-Controlled Deposition and Dissolution of Metals", in Modern Aspect of Electrochemistry, Vol. 7, Edited by B. E. CONWAY and J. O'M. BOCKRIS, pp. 256-268, Plenum Press, N.Y. 1972.										
NW	4	E. H. LYONS, "Fundamental Principles", in Modern Electroplating, 3 rd Edition, edited by F. A. LOWENHEIM, pp. 31-36, John Wiley & Sons, 1974.										
NW	5	J. JORNE, Challenges in Copper Interconnect Technology: Macro-Uniformity and Micro-Filling Power in Copper Electroplating of Wafers", in Semiconductor Fabtech - 11 th Edition, pp. 267-271, February 2000.										
NW	6	U. COHEN and G. TZANAVARAS, "Seed Layers and Cu Jets Plating for Interconnects Below 0.10 Micron", in the 17 th VLSI Multilevel Interconnection Conference (VMIC), pp. 21-26, Santa Clara, California, June 2000.										
EXAMINER									DATE CONSIDERED			
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.												